2. The output driver of claim 1 wherein the first drive block is connected in parallel with the second drive block.

3. The output driver of claim 1 wherein the first drive block includes one or more first drive transistors, the second drive block includes one or more second drive transistors, the first and second drive blocks having the same number of drive transistors, wherein the first drive transistors of the first drive block provide twice as much current as the second drive transistors of the second drive block.

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4. (Amended) The output driver of claim 1 wherein the first drive block includes [one] two or more first drive transistors, the first drive transistors being binary weighted with respect to each other to provide correspondingly weighted amounts of current in response to the MSB, the second drive block includes [one] two or more second drive transistors, the second drive transistors being binary weighted with respect to each other to provide correspondingly weighted amounts of current in response to the LSB, the first and second drive blocks having the same number of drive transistors.

5. The output driver of claim 3 wherein a set of current control signals enables and disables corresponding ones of the first and second drive transistors.

A2

6. (Amended) The output driver of claim 1 wherein binary signaling is used by setting the LSB [symbol] equal to zero.

7. The output driver of claim 3 wherein drive transistors are connected to an I/O pin, further comprising at least one constant current transistor connected to the I/O pin to provide a substantially continuous flow of current through the I/O pin to increase noise immunity.

8. An output driver to drive an output symbol representing two or more bits including a most significant bit (MSB) and a least significant bit (LSB), comprising:

a logic circuit to generate a set of transistor enable signals based on a state of the MSB and the LSB; and

a set of weighted transistors, each weighted transistor being responsive to one transistor enable signal of the set of transistor enable signals.

9. The output driver of claim 8 wherein the weighted transistors of the set of weighted transistors are weighted to compensate for gds distortion.

10. The output driver of claim 8 further comprising:

a set of current control transistors, responsive to current control signals, coupled to the set of weighted transistors, to adjust an amount of current supplied by the output driver.

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11. (Amended) The output driver of claim 8 [wherein each weighted transistor is differentially coupled to another correspondingly weighted transistor that is enabled to provide a continuous flow of current to increase noise immunity]

further comprising at least one current source coupled to at least one weighted transistor to provide a substantially continuous flow of current to reduce switching noise.

12. (Amended) An output driver to drive an output symbol representing two or more bits including a most significant bit (MSB) and a least significant bit (LSB), comprising:

a logic circuit to generate a set of transistor enable signals in accordance with a state of the MSB and LSB; and

a set of drive blocks, each drive block being responsive to one of the transistor enable signals, each drive block including a drive transistor responsive to one of the

transistor enable signals, at least a [of] subset of the drive blocks including a gds compensation transistor [resposive] responsive to one of the transistor enable signals, each gds compensation transistor having a predefined geometry to compensate for gds distortion.

13. (Amended) An output driver to drive an output symbol representing two or more bits including a most significant bit (MSB) and a least significant bit (LSB), comprising:

a logic circuit to generate a set of transistor enable signals in accordance with a state of the MSB and LSB; and

a set of drive blocks, each drive block including a set of drive transistors connected in series with a set of current-control transistors, the drive [tranisistors] transistors being responsive to one of the transistor enable signals, the set of current-control transistors being responsive to a set of current control signals, at least a [of] subset of the drive blocks including a set of gds compensation transistors connected in series with a set of gds-current-control transistors, the gds compensation transistors being [resposive] responsive to one of the transistor enable signals, and the gds-current-control transistors being responsive to gds-current-control signals.

14. The output driver of claim 13 wherein each set of drive transistors of the drive block are binary weighted.

15. (Amended) A bus receiver to receive an input symbol representing two or more bits including a most significant bit (MSB) and a least significant bit (LSB), comprising:

a MSB latching comparator to compare the input symbol to a MSB threshold voltage to generate a first binary output signal representing a state of the MSB;

a first LSB latching comparator to compare the input symbol to a first reference voltage to generate a second

binary output signal representing [the] a relationship between the input symbol and the first reference voltage;

a second LSB latching comparator to compare the input symbol to a second reference voltage to generate a third binary output signal representing [the] a relationship between the input symbol and the second reference voltage; and

a logic block to generate a fourth binary output signal representing a state of the LSB in accordance with the first, second and third binary output signals.

16. The bus receiver of claim 15 wherein the first, second and third latching comparators generate their respective binary output signals synchronized to a clock signal.

17. A bus receiver to receive an input symbol representing two or more bits, each bit being associated with at least one threshold voltage of a set of threshold voltages, comprising:

a most-significant-bit (MSB) receiver to receive the input symbol and provide an MSB logic signal representing a most-significant bit of the input symbol; and

a least-significant-bit (LSB) receiver to receive the input symbol and provide an LSB logic signal representing a least-significant bit of the input symbol.

18. The bus receiver of claim 17 wherein the MSB receiver and LSB receiver include:

at least one integrator to generate integration voltages on integration nodes by integrating charge in accordance with a voltage associated with the input symbol and one or more threshold voltages of the set of threshold voltages; and

at least one sense amplifier to receive the integration voltages of the at least one integrator to generate the logic signal of the respective receiver.

19. (Amended) The bus receiver of claim 17 wherein the MSB receiver and LSB receiver include:

at least one preamplifier to generate the input symbol by adjusting an unconditioned input symbol in accordance with [the] a relationship of the unconditioned input symbol to ranges of voltages defined by the voltages of the set of threshold voltages;

at least one integrator to generate integration voltages on integration nodes by integrating a charge in accordance with a voltage associated with the input symbol; and

at least one sense amplifier to receive the integration voltages of the at least one integrator to generate at least one logic signal representing a relationship of the input symbol to the one or more threshold voltages of the set of threshold voltages.

20. (Amended) A memory comprising:

an array of memory cells;

an address decoder;

a plurality of bus receivers to receive an address and also to receive input symbols, each input symbol representing a predetermined number of bits, each bit being associated with a range of voltage levels, a set of threshold voltages defining each range of voltage levels, comprising:

a most-significant bit (MSB) receiver to determine a MSB of the input symbol in accordance with a first threshold voltage of the set of threshold voltages; [and]

a least-significant bit (LSB) receiver to determine a LSB of the input symbol in accordance with second and third threshold voltages of the set of threshold voltages; and

an I/O circuit to store the MSB of the input symbol and LSB of the input symbol in a subset of memory cells of the array of memory cells.

21. The memory of claim 20 wherein the first threshold voltage is less than the second threshold voltage, and the first threshold voltage is greater than the third threshold voltage.

22. (Amended) The memory of claim 20,
wherein the MSB receiver includes:
at least one MSB integrator to generate integration voltages on integration nodes by integrating charge in accordance with a voltage of the input symbol with respect to the first threshold voltage; and
at least one MSB sense amplifier to receive the integration voltages of the at least one MSB integrator to generate at least one MSB logic signal representing [the] a relationship of the input symbol to the first threshold voltage; and
wherein the LSB receiver includes:
at least one LSB integrator to generate integration voltages on integration nodes by integrating charge associated with the voltage of the input symbol [output] with respect to the second and third threshold voltages; and
at least one LSB sense amplifier to receive the integration voltages of the at least one LSB integrator to generate at least one LSB logic signal representing [the] a relationship of the input symbol to the second and third threshold voltages,
wherein the I/O circuit stores signals representing the MSB logic signal and the LSB logic signal in the subset of memory cells of the memory array, as specified by the address.

23. (Amended) The memory of claim 20 wherein the MSB receiver includes:
at least one MSB preamplifier to generate a MSB preamplified signal in accordance with a relationship of the input symbol to a first threshold voltage of the set of threshold voltages;
at least one MSB integrator to accumulate charge to produce an output voltage in accordance with the MSB preamplified signal during an integration time interval

defined by a start integration timing event and an end integration timing event; and

at least one MSB sense amplifier to sample and convert the output voltage from the MSB integrator into a MSB logic signal representing a [MSB] state of the the MSB of the input signal; and

wherein the LSB receiver includes:

at least one LSB preamplifier to generate a LSB preamplified signal in accordance with a relationship of the input symbol to a second and third threshold voltage of the set of threshold voltages;

at least one LSB integrator to accumulate charge to produce an output voltage in accordance with the LSB preamplified signal during an integration time interval defined by a start integration timing event and an end integration timing event; and

at least one LSB sense amplifier to sample and convert the output voltage from the LSB integrator into an LSB logic signal representing a [LSB] state of the LSB of the input signal,

wherein the I/O circuit stores signals representing the MSB logic signal and the LSB logic signal in the subset of memory cells of the memory array, as specified by the address.

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24. The memory of claim 23 wherein the first threshold voltage is less than the second threshold voltage, and the first threshold voltage is greater than the third threshold voltage.

25. The memory of claim 20, further comprising:

a mode detection circuit to supply a PAM mode signal to cause the MSB receiver and LSB receiver to operate in either 4-PAM or 2-PAM mode.

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26. (Amended) A method [of correcting] for reducing errors in a multi-Pulse Amplitude Modulated (PAM) system including a

multi-PAM output driver and a multi-PAM receiver coupled via a data bus, comprising:

operating the multi-PAM output driver and the multi-PAM receiver at 4-PAM to exchange multi-PAM data on a bus;

[determining whether] detecting an error [occurred] in the multi-PAM data; and

operating the multi-PAM output driver and the multi-PAM receiver at 2-PAM to exchange binary data on the bus in response to detecting the error.

A 1 cont.

27. (Amended) The method of claim 26 wherein the multi-PAM output driver and the multi-PAM receiver are operated at a first [data] symbol rate, and further comprising:

reducing the first [data] symbol rate in response to [the] further error detection.

28. (Amended) The method of claim 27 further comprising:

measuring an error-free time; and

increasing the first [data] symbol rate when the error-free time equals a predetermined value.

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29. The method of claim 27 further comprising:

measuring an error-free time; and

operating the multi-PAM output driver and the multi-PAM receiver at 4-PAM when the error-free time equals a predetermined value.

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30. (Amended) A method [of correcting] for reducing errors in a multi-Pulse Amplitude Modulated (PAM) system, comprising:

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operating a multi-PAM output driver and a multi-PAM receiver at 4-PAM to exchange data on a bus, the data having a most-significant data bit and a least-significant data bit, wherein the multi-PAM output driver and the multi-PAM receiver transmit and receive an encoded multi-PAM symbol having a most-significant symbol bit [(MSB)] and a least-significant symbol bit [(LSB)], the most-significant data bit being

transmitted as the most-significant symbol bit, and the least-significant data bit being transmitted as the least-significant symbol bit;

[determining when] detecting an error [occurs] in the [data] multi-PAM symbol; and

[switching the MSB and LSB when an error occurs] transmitting the least-significant data bit as the most-significant symbol bit and the most-significant data bit as the least-significant symbol bit in response to the error.

31. (Amended) A bus system comprising:

a signal line;

a first output driver to transmit a first data signal on the signal line;

a second output driver to transmit a second data signal on the signal line simultaneously with the first data signal such that the first and second data signals are superimposed to produce a superimposed data signal on the signal line, the superimposed data signal having a plurality of voltage levels representing the combinations of the simultaneously transmitted data signals;

a first receiver to receive the superimposed data signal, to determine a digital representation of the superimposed data signal, and [identifying] identify the data signal transmitted by the second output driver from the superimposed data signal; and

a second receiver to receive the superimposed data signal, to determine a digital representation of the superimposed data signal, and [identifying] identify the data signal transmitted from the first output driver from the superimposed data signal.

32. (Amended) A memory system comprising:

a bus having a plurality of signal lines [:] ;

a plurality of output drivers to drive an output symbol representing a predetermined number of bits including a most

significant bit (MSB) and a least significant bit (LSB) on a first subset of the signal lines; and

a plurality of receivers, each receiver to receive the output symbol from a respective signal line as an input symbol, each input symbol representing the predetermined number of bits, the receivers outputting a plurality of logic signals representing the state of the MSB and LSB of the input symbol.

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33. The memory system of claim 32 wherein the memory system is operated as a 4-PAM system such that the output symbol has an MSB and an LSB; and the memory system is operated as a 2-PAM system by setting the LSB of the output symbol to zero to generate a 2-PAM symbol.

34. The memory system of claim 32 wherein the first set of signal lines include control signal lines and data signal lines, the control signal lines being 2-PAM, and the data signal lines being 4-PAM.

35. The memory system of claim 32 wherein the memory system is responsive to a mode signal to switch between 4-PAM and 2-PAM.

36. The memory system of claim 35 wherein the mode signal is determined by a hardware setting.

37. The memory system of claim 32 wherein the memory system is responsive to detected errors to switch between 4-PAM and 2-PAM.

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38. (Amended) A memory system comprising:

a bus having a plurality of signal lines;

a first subset of the signal lines being coupled to a plurality of output drivers, each output driver to drive an output symbol representing two bits including a most

significant bit (MSB) and a least significant bit (LSB) on the signal line, each output driver including:

a first drive block to generate a MSB symbol component representing the MSB; and

a second drive block to generate an LSB symbol component representing the LSB, the LSB symbol component being combined with the MSB symbol component to provide the output symbol;

a second subset of the signal lines, including the first subset of signal lines, being coupled to a plurality of bus receivers to receive an address and [the output symbols, the received output symbols being] input symbols, each input symbol representing a predetermined number of bits, each bit being associated with a distinct range of voltage levels, a set of threshold voltages defining each distinct range of voltage levels, each bus receiver including:

a most-significant bit (MSB) receiver to determine the MSB of a respective one of the input symbols [symbol] based on a first threshold voltage of the set of threshold voltages; and

a least-significant bit (LSB) receiver to determine the LSB of a respective one of the input symbols [symbol] based on second and third threshold voltages of the set of threshold voltages.

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39. A method of operating a multi-drop bus using multi-level signals, comprising:

transmitting an output symbol representing at least two bits including a most significant bit (MSB) and a least significant bit (LSB);

receiving the output symbol, the received output symbol being an input symbol;

generating integration voltages by integrating charge on at least one integration node in accordance with a state of the input symbol; and

determining the MSB and the LSB in accordance with the integration voltages.

40. An apparatus for transmitting data on a multi-drop bus using multi-level signals, comprising:

means for transmitting an output symbol representing at least two bits including a most significant bit (MSB) and a least significant bit (LSB);

means for receiving the output symbol, the received output symbol being an input symbol;

means for generating integration voltages by integrating charge on at least one integration node in accordance with a state of the input symbol; and

means for determining the MSB and the LSB in accordance with the integration voltages.

NEW CLAIMS:

41. (New) An apparatus for receiving multi-level signals, the apparatus comprising:

a bus comprising a plurality of signal lines to carry said multi-level signals comprising at least a first signal and a second signal, said plurality of signal lines having at least a first signal line and a second signal line carrying said first signal and said second signal respectively, wherein said multi-level signals have one of at least three (3) distinct signal levels;

a plurality of multi-level receivers coupled to said plurality of signal lines, said plurality of multi-level receivers comprising a first multi-level receiver and a second multi-level receiver, wherein said first multi-level receiver is coupled to said first signal line to receive said first signal and said second multi-level receiver is coupled to said second signal line to receive said second signal;

said first multi-level receiver generating a first output; and

said second multi-level receiver generating a second output, wherein said first and second outputs collectively represent more than two (2) digital bits.

42. (New) The apparatus of claim 41 wherein said bus is a multi-drop bus.

43. (New) The apparatus of claim 42 wherein said multi-drop bus is terminated.

44. (New) The apparatus of claim 41 wherein said plurality of signal lines are terminated with a terminating resistor.

45. (New) The apparatus of claim 41 wherein said multi-level signals have one of at least four (4) distinct levels.

46. (New) The apparatus of claim 41 wherein said at least three distinct signal levels are voltage levels.

47. (New) The apparatus of claim 41 wherein said at least three distinct signal levels are current levels.

48. (New) The apparatus of claim 41 wherein said first multi-level receiver and said second multi-level receiver comprise a first integrator and a second integrator respectively.

49. (New) The apparatus of claim 48 wherein said first multi-level receiver comprises a first sampling circuit to sample said first signal between transitions of said first signal.

50. (New) The apparatus of claim 49 wherein said second multi-level receiver comprises a second sampling circuit to sample said second signal between transitions of said second signal.

A10 Cont.

51. (New) The apparatus of claim 50 wherein said first sampling circuit and said second sampling circuit sample in response to a clock transition.

52. (New) The apparatus of claim 41 wherein said first multi-level receiver and said second multi-level receiver comprise a first decoder and a second decoder, respectively, to decode said first signal and said second signal on a clock transition.

53. (New) The apparatus of claim 52 wherein said multi-level signals collectively represent a data value.

54. (New) The apparatus of claim 52 wherein said multi-level signals collectively represent a control value.

55. (New) The apparatus of claim 54 wherein said control value represents an address.

56. (New) The apparatus of claim 54 wherein said control value represents a read command.

57. (New) The apparatus of claim 54 wherein said control value represents a write command.

58. (New) An apparatus for transmitting multi-level signals comprising:

a bus comprising a plurality of signal lines to carry said multi-level signals comprising at least a first signal and a second signal, said plurality of signal lines having at least a first signal line and a second signal line carrying said first signal and said second signal respectively, wherein said multi-level signals have one of at least three (3) distinct signal levels; and

a plurality of multi-level output drivers coupled to said plurality of signal lines, said plurality of multi-level

output drivers comprising a first multi-level output driver and a second multi-level output driver,

said first multi-level output driver outputting said first signal onto said first signal line; and

said second multi-level output driver outputting said second signal onto said second signal line, wherein said first and second signals collectively represent more than two (2) digital bits.

59. (New) The apparatus of claim 58 wherein said multi-level signals have one of at least four (4) distinct levels.

60. (New) The apparatus of claim 58 wherein said at least three distinct signal levels are voltage levels.

61. (New) The apparatus of claim 58 wherein said at least three distinct signal levels are current levels.

62. (New) The apparatus of claim 58 wherein said plurality of multi-level output drivers are current drivers.

63. (New) The apparatus of claim 58 wherein said multi-level signals collectively represent a data value.

64. (New) The apparatus of claim 58 wherein said multi-level signals collectively represent a control value.

65. (New) The apparatus of claim 64 wherein said control value represents an address.

66. (New) The apparatus of claim 64 wherein said control value represents a read command.

67. (New) The apparatus of claim 64 wherein said control value represents a write command.

68. (New) A multi-level signaling system comprising:

a signaling path comprising a plurality of signal lines including a first signal line and a second signal line;

a plurality of multi-level output drivers coupled to said signaling path to output thereon multi-level signals comprising at least a first signal and a second signal, wherein said multi-level signals have one of at least three (3) distinct signal levels;

said plurality of multi-level output drivers comprising a first multi-level output driver and a second multi-level output driver, wherein said first multi-level output driver outputs said first signal onto said first signal line and said second multi-level output driver outputs said second signal onto said second signal line, wherein said first signal and said second signal collectively represent more than two (2) digital bits;

a plurality of multi-level receivers coupled to said signaling path to receive therefrom said multi-level signals, said plurality of multi-level receivers comprising a first multi-level receiver and a second multi-level receiver, wherein said first multi-level receiver is coupled to said first signal line to receive said first signal and said second multi-level receiver is coupled to said second signal line to receive said second signal;

said first multi-level receiver generating a first output; and

said second multi-level receiver generating a second output, wherein said first output and said second output collectively represent more than two (2) digital bits.

A10 cont.

69. (New) The apparatus of claim 68 wherein said signaling path is a multi-drop bus.

70. (New) The apparatus of claim 69 wherein said multi-drop bus is terminated.

71. (New) The apparatus of claim 68 wherein said plurality of signal lines are terminated with a terminating resistor.

72. (New) The apparatus of claim 68 wherein said at least three distinct signal levels are voltage levels.

73. (New) The apparatus of claim 68 wherein said at least three distinct signal levels are current levels.

74. (New) The apparatus of claim 68 wherein said first multi-level receiver and said second multi-level receiver comprise a first integrator and a second integrator respectively.

A10 cont.

75. (New) The apparatus of claim 74 wherein said first multi-level receiver comprises a first sampling circuit to sample said first signal between transitions of said first signal.

76. (New) The apparatus of claim 75 wherein said second multi-level receiver comprises a second sampling circuit to sample said second signal between transitions of said second signal.

77. (New) The apparatus of claim 76 wherein said first sampling circuit and said second sampling circuit sample in response to a clock transition.

78. (New) The apparatus of claim 68 wherein said first multi-level receiver and said second multi-level receiver comprise a first decoder and a second decoder respectively to decode said first signal and said second signal on a clock transition.

79. (New) The apparatus of claim 68 wherein said plurality of multi-level output drivers are current drivers.

80. (New) A memory device comprising:

a signaling path carrying multi-level signals comprising at least a first signal and a second signal, said signaling path comprising a plurality of signal lines including a first signal line and a second signal line carrying said first signal and said second signal respectively, wherein said multi-level signals have one of at least three (3) distinct signal levels, and said first signal and said second signal collectively represent more than two (2) digital bits;

a plurality of multi-level receivers coupled to said signaling path to receive therefrom said multi-level signals, said plurality of multi-level receivers comprising a first multi-level receiver and a second multi-level receiver, wherein said first multi-level receiver is coupled to said first signal line to receive said first signal and said second multi-level receiver is coupled to said second signal line to receive said second signal;

said first multi-level receiver and said second multi-level receiver generating at least a first digital bit and a second digital bit based on said first signal and said second signal; and

an array of memory cells coupled to said plurality of multi-level receiver circuits to store said first digital bit and said second digital bit.

A10 Cont.

81. (New) The apparatus of claim 80 wherein said signaling path is a multi-drop bus.

82. (New) The apparatus of claim 81 wherein said multi-drop bus is terminated.

83. (New) The apparatus of claim 80 wherein said first multi-level receiver and said second multi-level receiver comprise a first integrator and a second integrator respectively.

84. (New) The apparatus of claim 83 wherein said first multi-level receiver comprises a first sampling circuit to sample said first signal between transitions of said first signal.

85. (New) The apparatus of claim 84 wherein said second multi-level receiver comprises a second sampling circuit to sample said second signal between transitions of said second signal.

86. (New) The apparatus of claim 85 wherein said first sampling circuit and said second sampling circuit sample in response to a clock transition.

87. (New) The apparatus of claim 80 wherein said first multi-level receiver and said second multi-level receiver comprise a first decoder and a second decoder respectively to decode said first signal and said second signal on a clock transition.

88. (New) A memory device comprising:

an array of memory cells;

a plurality of multi-level output drivers coupled to said array of memory cells to receive a data value therefrom, said data value comprising N bits, where N is an integer; and

said plurality of multi-level output drivers being structured to output M signals representative of said data value onto a signaling path, where M is an integer less than N, said M signals having one of at least three (3) distinct signal levels.

89. (New) The apparatus of claim 88 wherein said at least three distinct signal levels are voltage levels.

90. (New) The apparatus of claim 88 wherein said at least three distinct signal levels are current levels.

91. (New) The apparatus of claim 88 wherein said plurality of multi-level output drivers are current drivers.

92. (New) The apparatus of claim 88 wherein said M signals collectively represent a data value.

93. (New) The apparatus of claim 88 wherein said M signals collectively represent a control value.

94. (New) A memory controller for transmitting M1 signals to a memory device and receiving M2 signals from said memory device, where said M1 and M2 are integers, said memory controller comprising:

a plurality of multi-level output drivers to output to said memory device said M1 signals representative of a first data value comprising N1 bits, where N1 is an integer greater than M1, said M1 signals having one of at least three distinct signal levels; and

a plurality of multi-level receivers to receive from said memory device said M2 signals representative of a second data value comprising N2 bits, where N2 is an integer greater than M2, said M2 signals having one of said at least three (3) distinct signal levels.

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95. (New) The apparatus of claim 94 wherein said plurality of multi-level receivers comprise a plurality of integrators.

96. (New) The apparatus of claim 95 wherein said plurality of multi-level receivers comprise a plurality of sampling circuits to sample said M2 signals between transitions of said M2 signals.

97. (New) The apparatus of claim 96 wherein said plurality of sampling circuits sample in response to a clock transition.

98. (New) The apparatus of claim 94 wherein said plurality of multi-level receivers comprise a plurality of decoders to decode said M2 signals.

99. (New) The apparatus of claim 94 wherein said plurality of multi-level output drivers are current drivers.

100. (New) The apparatus of claim 94 wherein said at least three distinct signal levels are voltage levels.

101. (New) The apparatus of claim 94 wherein said at least three distinct signal levels are current levels.

A10 Cont.

102. (New) A memory system comprising:

a signaling path;

a memory device having a plurality of multi-level output drivers coupled to said signaling path to output thereon M signals representative of a data value comprising N bits, where M and N are integers and M is less than N, said M signals having one of at least three (3) distinct signal levels; and

a memory controller having a plurality of multi-level receivers coupled to said signaling path to receive therefrom said M signals, decode said M signals and produce an output representative of said data value.

103. (New) The apparatus of claim 102 wherein said signaling path is a multi-drop bus.

104. (New) The apparatus of claim 102 wherein said plurality of multi-level receivers comprise a plurality of integrators.

105. (New) The apparatus of claim 104 wherein said plurality of multi-level receivers comprise a plurality of sampling

circuits to sample said M signals between transitions of said M signals.

106. (New) The apparatus of claim 105 wherein said plurality of sampling circuits sample in response to a clock transition.

107. (New) The apparatus of claim 102 wherein said plurality of multi-level receivers comprise a plurality of decoders to decode said M signals.

108. (New) The apparatus of claim 107 wherein said multi-level signals collectively represent a data value.

109. (New) The apparatus of claim 107 wherein said multi-level signals collectively represent a control value.

110. (New) The apparatus of claim 102 wherein said at least three distinct signal levels are voltage levels.

111. (New) The apparatus of claim 102 wherein said at least three distinct signal levels are current levels.

112. (New) The apparatus of claim 102 wherein said plurality of multi-level output drivers are current drivers.

A/O cancel.

REMARKS

Please enter the amendment After entry of this amendment, the pending claims are: claims 1-112.

The change in the specification on page 84, line 12, is to correct a typographical error.